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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/771,473	02/05/2004	Takahide Shigeno	Q79746	2960

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EXAMINER	
ETTEHADIEH, ASLAN	

ART UNIT	PAPER NUMBER
2611	

MAIL DATE	DELIVERY MODE
06/15/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/771,473	SHIGENO, TAKAHIDE	
	Examiner	Art Unit	
	Aslan Ettehadieh	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☒ Claim(s) *4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 10/771473, filed on 02/05/2004.

NOTE

Please note that all references made herein to the instant application are made with respect to paragraphs of U.S. Patent Application Publication No. 2004/0160289, the publication corresponding to the instant application.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 – 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasuhiro (JP 07-170167; which is applicant own admitted prior art, see paragraph 6 and IDS) in view of Tenshiyuu (JP 10-173510; which is applicant own admitted prior art, see IDS).

4. Regarding claim 1, Yasuhiro discloses a signal relay circuit for relaying a digital signal transmitted from a signal generating unit to a signal receiving unit and having a first potential level and a second potential level that is higher than said first potential level, said circuit comprising: a capacitor connected between said signal generating unit and said signal receiving unit for receiving digital signal, eliminating a DC component from said digital signal as received, and outputting the digital signal, from which said DC component is eliminated, to said signal receiving unit as a restored digital signal (figure 1 element 1, paragraphs 2, 13; where the signal generating unit is prior to the capacitor element of figure 1); a first resistor having one terminal connected to a power supply which pulls up the potential of said restored digital signal as received from said capacitor and the other terminal connected to a relay point between said capacitor and said signal receiving unit (figure 1 element 5; paragraphs 1, 5, 13, 19 – 22); and a second resistor having one terminal connected to said relay point and the other terminal connected to a ground potential (figure 1 element 7; paragraphs 1, 5, 13, 19 – 22). Yasuhiro is not explicit about having a resistance value with which a current flowing through said first resistor is smaller than an output current of said first potential level from said signal generating unit and having a resistance value with which a current flowing through said second resistor is smaller than an output current from said signal generating unit having said second potential level, however, Yasuhiro discloses the first resistance is connected to a high potential side of the power source and the second resistance is connected to the low voltage side of the power source.

In the same field of endeavor, however, Tenshiyuu discloses having a resistance value with which a current flowing through said first resistor is smaller than an output current of said first potential level from said signal generating unit and having a resistance value with which a current flowing through said second resistor is smaller than an output current from said signal generating unit having said second potential level (figure 1, paragraph 7, 8, 10, 11).

Therefore it would have been obvious to one skilled in the art at the time of invention was made to use having a resistance value with which a current flowing through said first resistor is smaller than an output current of said first potential level from said signal generating unit and having a resistance value with which a current flowing through said second resistor is smaller than an output current from said signal generating unit having said second potential level as taught by Tenshiyuu in the system of Yasuhiro to provide stability (paragraph 20).

5. Regarding claim 2, Tenshiyuu further discloses a the resistance value of said second resistor is selected in order that the maximum value of said first potential level is not exceeded by the voltage drop due to a leakage current that is flowing from said signal receiving unit into said ground potential (paragraph 11).

6. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yasuhiro (JP 07-170167; which is applicant own admitted prior art, see paragraph 6 and IDS) in

view of Tenshiyuu (JP 10-173510; which is applicant own admitted prior art, see IDS) in further view of Orii (US 2001/0026160).

7. Regarding claim 3, Yasuhiro is silent about the power voltage of said signal receiving unit is equal to that of said power supply, the resistance value of said first resistor is equal to that of said second resistor, Yasuhiro discloses the electronic equipment can have many power supplies or a single power supply (paragraph 1) and the first resistance is connected to the power source (paragraph 13).

In the same field of endeavor, however, Orii discloses the power voltage of said signal receiving unit is equal to that of said power supply, the resistance value of said first resistor is equal to that of said second resistor (paragraphs 12 – 14, figure 1 element 11).

Therefore it would have been obvious to one skilled in the art at the time of invention was made to use the power voltage of said signal receiving unit is equal to that of said power supply, the resistance value of said first resistor is equal to that of said second resistor as taught by Orii in the system of Yasuhiro to accurately convert the signal (paragraphs 9 – 10).

Allowable Subject Matter

8. Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Other prior art cited

9. The prior art made of record and not relies upon is considered pertinent to applicant's disclosure.

10. Yamamoto (US 2002/0070807) discloses a system of relevance to claims 1 – 4 (abstract, figures 1 and 6).

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aslan Ettehadieh whose telephone number is (571) 272-8729. The examiner can normally be reached on Monday - Friday, 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on (571) 272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Aslan Ettehadieh
Examiner
Art Unit 2611

David Payne
DAVID C. PAYNE
SUPERVISORY PATENT EXAMINER